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Memristors based on TiO_x/HfO_x or AlO_x/HfO_x Multilayers with Gradually Varied Thickness

Binfeng Yin, Yongzhi Wang, Guancai Xie, Beidou Guo, and Jian Ru Gong**

As a fourth fundamental two-terminal circuit element, memristors have received great research interest as resistive random access memory (RRAM). Herein, a new memristor structure based on TiO_x/HfO_x or AlO_x/HfO_x multilayers with gradually varied thickness as the switching material is fabricated. The devices show forming-free, self-compliance, reliable multilevel resistive switching, and low switching voltage properties, and are promising for applications in future advanced integrated circuits.

1. Introduction

Memristors have been considered as one of the most promising candidates in the next generation of nonvolatile memory.[1–4] In particular, HfO_2-based memristors have attracted great interest due to their fast switching speed, low power consumption, and compatibility with complementary metal–oxide–semiconductor technology.[5–7] However, the application of HfO_2-based memristors is still facing many challenges, such as complicated forming process, overshoot current, and insufficient storage capacity. To address these issues, many efforts have been made. For example, forming-free devices have been demonstrated by metal doping.[8,9] The annealing procedure or the complicated device structure has been adopted for compliance current to prevent the overshoot current.[10,11] Also, multilevel storage capability have been achieved through a bilayer structure.[12,13] Unfortunately, simultaneous realization of the forming-free, self-compliance, and multilevel storage capability characteristics, which is necessary to meet the demands of practical applications for memristors, has been not reported for HfO_2-based memristors so far.

In this letter, we reported a new type of memristor structure consisting of TiO_x/HfO_x or AlO_x/HfO_x multilayer with gradually varied thickness. As compared with memristors based on a single layer or bilayer structure, the memristors with the multilayer structure have the following advantages. First, the more interfaces in multilayer structures can be utilized to modulate the performance of oxide-based memristors through manipulating the migration of oxygen ions and vacancies.[14,15] Second, multilayer structures are feasible to achieve the multilevel storage capability.[16] Third, multilayer structures can also play a key role in tuning the switching voltage and the conductance of the devices.[17] At the same time, the multilayer structure with gradually varied thickness, in our work, also has the following features. First, the thin layers in the multilayer structure would trigger a low-electric-filed-induced switching operation that may eliminate the forming process, whereas the thick layers with different thicknesses are designed to avoid the breakdown of the whole device at larger voltages. Second, the HfO_x layers especially the thick ones can act as the series resistors to limit the overshoot current for self-compliance current. Finally, the thin layer in the multilayer structure can, in principle, achieve low SET current/voltage as compared with the thicker ones in a bilayer structure.[18] Our experiments demonstrated that the memristors with such a structure showed forming-free, self-compliance, multilevel storage properties, and low switching voltage, which are conducive to promote the development of high-density integrated and low-cost circuits.

2. Experimental Section

First, a 100 nm Ti bottom electrode was defined by photolithography and deposited by radio frequency (RF) magnetron sputtering on the Si/SiO_2 substrate. Then, a second photolithography was performed to define the pattern of the memristor crossbar array, followed by thermal atomic layer deposition (ALD) of thickness varying components of the TiO_x/HfO_x or AlO_x/HfO_x multilayer. In detail, the multilayer TiO_x/HfO_x with a total thickness of about 8 nm was deposited at 180 °C by six ALD deposition rounds via varying the ALD cycles of each material, resulting in the gradually varied thickness of each material, as listed in **Table 1**. The annealing process was performed at 400 °C for 10 min in nitrogen atmosphere. Finally, a 60 nm Pt top electrode was prepared by RF magnetron sputtering. The memristor crossbar structure is shown in **Figure 1**a with a typical device area of $10 \times 10\ \mu m^2$, which is schematically shown in Figure 1b. A similar $Ti/(AlO_x/HfO_x)_n/Pt$ memristor with the total thickness of 8 nm was also prepared (Table 1). The electronic properties of

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Table 1. Film deposition thickness (nm) of the Ti/$(TiO_x/HfO_x)_n$/Pt and Ti/$(AlO_x/HfO_x)_n$/Pt memristors.

Film	$N(1)$	$N(2)$	$N(3)$	$N(4)$	$N(5)$	$N(6)$
TiO_x/HfO_x	1.35/0	1.08/0.24	0.81/0.48	0.54/0.72	0.27/0.96	0/1.68
AlO_x/HfO_x	1.68/0	0.96/0.24	0.72/0.48	0.48/0.72	0.24/0.96	0/1.68

the devices were measured using an FS-Pro semiconductor characterization system in air, and the top electrode Pt was grounded.

3. Results and Discussion

For the Ti/$(TiO_x/HfO_x)_n$/Pt device before annealing, a forming process involving a voltage about 2 V being applied to the bottom electrode Ti is required to activate resistive-switching operation (**Figure 2**a), subsequently represents typical I–V characteristics in the Ti/$(TiO_x/HfO_x)_n$/Pt device, revealing a typical pinched hysteresis loop sign of the memristor device. The I–V characteristics of the Ti/TiO_x(4 nm)/HfO_x(4 nm)/Pt device with a bilayer structure were also tested. The device has no obvious switch ratio (about 2), and its SET current is ten times higher than that of the Ti/$(TiO_x/HfO_x)_n$/Pt memristor before annealing, as shown in Figure 2b. Interestingly, the annealed Ti/$(TiO_x/HfO_x)_n$/Pt memristor reveals the pinched hysteresis loop without the forming process, as shown in **Figure 3**a. The Ti/$(TiO_x/HfO_x)_n$/Pt memristor shows a set voltage (V_{SET}) of 1 V, which is obviously lower than previous reported memristors with a bilayer TiO_x/HfO_2 (1.52 V)[18] or TiO_2/HfO_2 (less than −2 V)[19] structure, thus verifying the advantage of the memristors with our structure in achieving low V_{SET}. Furthermore, the multilevel storage property was also demonstrated for this memristor by applying different reset voltages (V_{RESET}), which can be observed as the two different resistance state levels (state 1 and state 2). Among them, the V_{RESET} sweep ranges of state 1 and state 2 are 0 to −2 V and 0 to −2.5 V, respectively, which are applied to the memristor. As previous reports[20,21] have demonstrated the good retention characteristics (generally longer than 10^3 s) of multilevel states in memristors based on multilayer oxide switching layers, our present work mainly focuses on the multilevel storage feature of our designed memristor, and only the stability of storage state 1 was measured as an example to confirmed its endurance. Figure 3b shows the typical dc retention data for both high-resistance state (HRS) and low-resistance state (LRS) up to 10^3 s at room temperature under a reading voltage of 0.2 V, indicating the good data retention of our memristor. The endurance of this memristor was also tested for five consecutive cycles, as shown in Figure 2c, to measure the reliability of the device. This measurement shows the well-resolved HRS and LRS states over five cycles with an average on/off ratio of 11.2, which can conform to the application requirement of resistive random access memory (RRAM).[13] In addition, we checked the variability of our devices by measuring five different devices, as shown in Figure 2d. A statistical analysis gives mean HRS and LRS of the devices to be 1.8×10^5 and 1.1×10^4, respectively. Compared with LRS, HRS shows larger variability in our case. However, comprehensive reliability characteristics of the memristor are still need to be further investigated, and better performance can be expected after the optimization of materials and their fabrication method, and testing protocol.

To describe the operating principle of the optimized device, schematic diagrams of the formation and rupture process of conductive filaments are proposed based on previous reports on memristors with multilayer oxides.[20,21] The initial state of the device is schemed in **Figure 4**a. It has been widely recognized that the TiO_x and HfO_x dielectric layers prepared by ALD are amorphous due to the presence of plentiful oxygen vacancies (V_O).[22] When a forward bias is applied to the Ti bottom electrode, oxygen ions (O^{2-}) will move toward the Ti electrode and accumulate at the bottom Ti/TiO_x interface (Figure 4b). During the O^{2-} movement, the HfO_x layers can act as series resistors and play an important role in the self-compliance characteristics of the device.[13] Once the bias reaches the SET voltage, tapered conductive filaments will be formed in TiO_x layers, and the different HfO_x layers are mainly in the state with the formation of narrow conductive filaments,[13] and the device, thus, changes from HRS to LRS when V_O conducting filaments connect Pt and Ti. In our structure, the ultrathin layer thickness ranging from 0.24 to 1.68 nm makes it conducive to the forming-free and low SET current/voltage characteristics as compared with the thicker sublayers in a uniform bilayer structure with

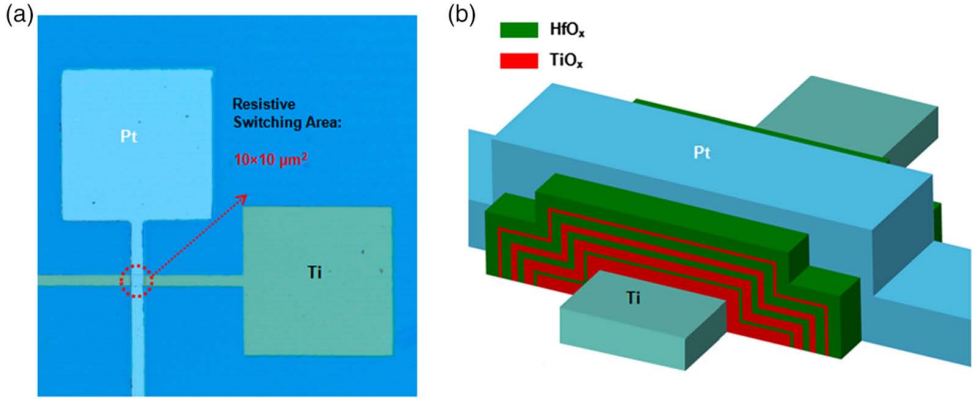

Figure 1. a) Optical microscopy image of the Ti/$(TiO_x/HfO_x)_n$/Pt memristor and the resistive-switching area. b) The schematic diagram of the Ti/$(TiO_x/HfO_x)_n$/Pt memristor.

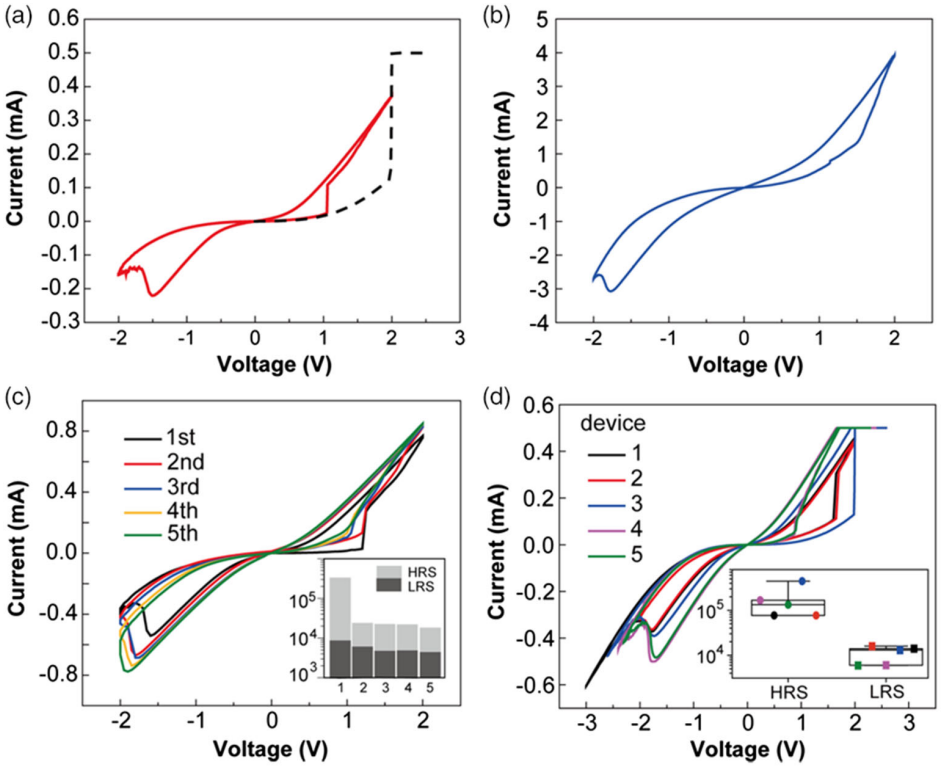

Figure 2. a) Forming process (black line) and *I–V* characteristic curve (red line) of the Ti/$(TiO_x/HfO_x)_n$/Pt memristor before annealing. b) *I–V* characteristic curve of the Ti/(TiO_x/HfO_x)/Pt device. c) *I–V* characteristic curve of the Ti/$(TiO_x/HfO_x)_n$/Pt memristor over five consecutive cycles and the corresponding values of HRS and LRS. d) *I–V* characteristic curve of five different Ti/$(TiO_x/HfO_x)_n$/Pt memristors and the corresponding statistical resistance at HRS and LRS.

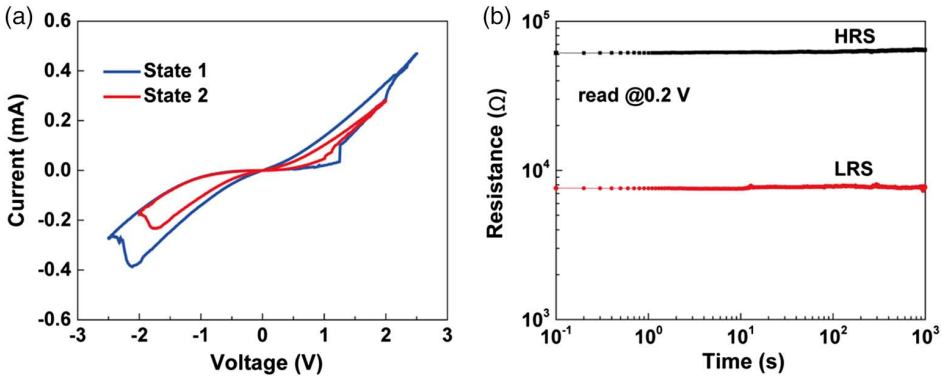

Figure 3. a) *I–V* characteristic curve and b) stability testing of the Ti/$(TiO_x/HfO_x)_n$/Pt memristor after annealing.

the same total thickness (Figure 1), and the multilayer is beneficial to the formation of the multistate.[23] In addition to that, the amorphous dielectric layers can transform from total disorder to partial order after annealing, which makes it easy to form V_O conductive filaments, so that the SET process in our device does not require the forming process. When a reverse bias is applied to the Ti bottom electrode, O^{2-} accumulated at the Ti/TiO_x interface is driven to combine with V_O in the bottom TiO_x layer, leading to the rupture of the filament,[24] and thus, the device turns to HRS, as shown in Figure 4c. It should be noticed that the above-mentioned mechanism is based on previous reports on various oxide-based memristors including those with bilayer oxides[5,13,19] and trilayer oxides.[20,21] The exact mechanism is still need to be investigated by further characterization such as in situ transmission electron microscopy (TEM).

To demonstrate the universality of our proposed switching layer structure for achieving forming-free, self-compliance, and multilevel storage memristors, similarly, we also fabricated a Ti/$(AlO_x/HfO_x)_n$/Pt memristor with the AlO_x/HfO_x multilayer. *I–V* characteristic curve of the memristor also shows the pinched hysteresis loop (**Figure 5**a). In the sweep voltage range of −0.8 to 0.8 V, the device shows ultralow SET and RESET voltages, with

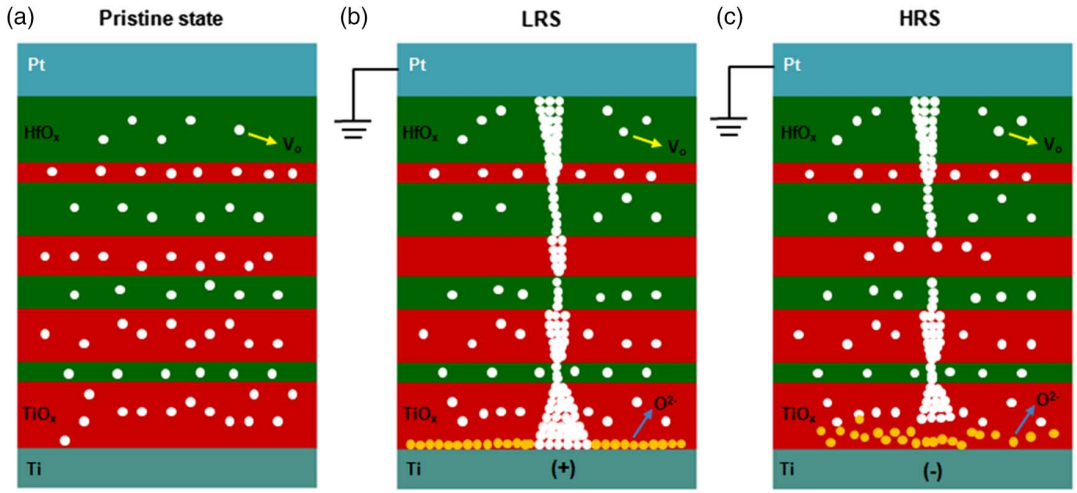

Figure 4. a–c) Schematic diagrams for the mechanism of the resistive-switching process in the Ti/$(TiO_x/HfO_x)_n$/Pt memristor after annealing: a) pristine state, b) LRS, and c) HRS.

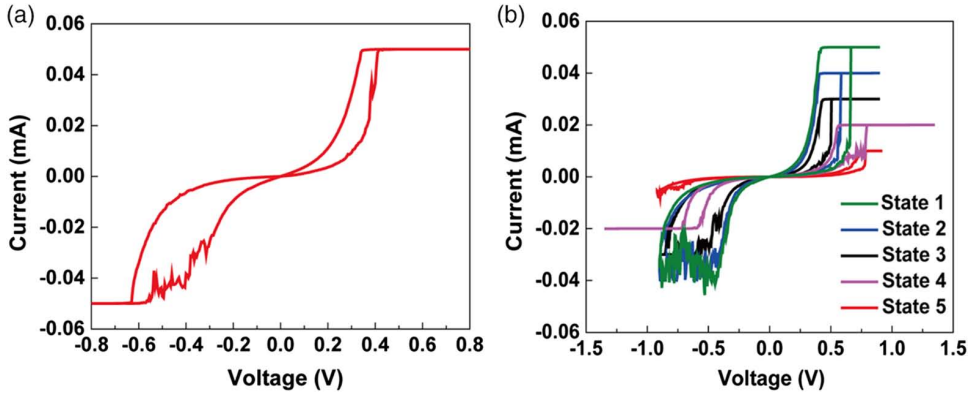

Figure 5. a) *I–V* characteristic curve of the Ti/$(AlO_x/HfO_x)_n$/Pt memristor. b) Multistate storage characteristics of the Ti/$(AlO_x/HfO_x)_n$/Pt memristor.

the values of ≈0.38 and approximately −0.3 V, respectively, when using the compliance current of 50 μA. Furthermore, the device exhibits the forming-free property without the annealing process. As shown in Figure 5b, five stable storage states for the Ti/$(AlO_x/HfO_x)_n$/Pt memristor were achieved by increasing the compliance current from 10 to 50 μA with a 10 μA increment. The more storage states for the Ti/$(AlO_x/HfO_x)_n$/Pt memristor as compared with the Ti/$(TiO_x/HfO_x)_n$/Pt memristor can be due to the larger on/off ratio of the former devices.[25] To avoid the breakdown of the device, we did not continue to increase the clamping current. The abovementioned results, thus, verify the universality of memristors with such switching layer structure.

In our work, all the devices show the SET and RESET voltages below 2 V benefiting from the less than 10 nm dielectric layer, and they also show self-compliance property. The Ti/$(AlO_x/HfO_x)_n$/Pt device has a very low SET voltage and verifies the feasibility of our design idea—thickness varying components of TiO_x/HfO_x or AlO_x/HfO_x as the switching layer. We believe that, after further optimization on material selection, dielectric layer thickness, and preparation process, devices based on such components layer structure will have great potential in the field of high-density storage devices.

4. Conclusion

We have fabricated a novel memristor based on multilayer TiO_x/HfO_x or AlO_x/HfO_x with gradually varied thickness, which simultaneously realizes the properties of forming-free, multilevel resistive switching, low switching voltage, and self-compliance. The possible switching mechanism is proposed. This structure can have great potentials for application in high-density storage devices and low-energy electronics.

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Conflict of Interest

The authors declare no conflict of interest.

Data Availability Statement

Research data are not shared.

Keywords

forming-free, HfO_x, memristors, multilayers, self-compliance

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